REMARKS

This amendment responds to the office action mailed February 2, 2007. In the office action the Examiner:

- rejected claims 1-42 as being indefinite under 35 U.S.C. 112, second paragraph;
- rejected claims 1-4, 21-26, 34, 35 and 42 under 35 U.S.C. 102(e) as being anticipated Desai (US 6,862,296); and
- rejected claims 5, 13, 14, 18-20 and 39-41 under 35 U.S.C. 103(a) as being unpatentable over Desai (US 6,862,296).

After entry of this amendment, the pending claims are: claims 1-42.

CLAIM AMENDMENTS

Claim 27 has been amended to clarify that the previously claimed "clock cycle detector" is a "clock duty cycle detector."

CLAIM REJECTIONS – 35 U.S.C. § 112

The Examiner rejected claims 1-42 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The following remarks, addressing the rejections under 35 U.S.C. § 112, second paragraph, are directed to specification support for claim elements and clarity of the claim limitations, and are not directed to the scope of these claim elements. Claim scope and novelty are addressed separately.

Regarding claim 1, the Examiner states that the drawings do not disclose a circuit for "detecting a duty cycle of a data signal." The Examiner states that the phrase "detected duty cycle" is indefinite because it could refer to either the duty cycle of data signal or of the system clock. The Examiner states that the phrase "detecting a duty cycle of a data signal" is misdescriptive. The Examiner further states that the duty cycle detector 250-A shown in Figure 2D is merely a level detector and cannot detect a duty cycle.

Applicants first note that support for every limitation in claim 1 is contained in the flow diagram of Figure 3. In addition, Figure 2B shows a duty cycle detector 228 that detects the duty cycle of a data signal 226. *See* Specification ¶ [0034] ("A duty cycle detector

228 detects the duty cycle of the data signal 226."). In some embodiments, the duty cycle detector 228 of Figure 2B is implemented as a duty cycle detector 250-A of Figure 2D, which is "suitable for detecting the duty cycle . . . of a periodic data signal." *Id.* ¶ [0038]. The duty cycle detector 250-A compares the detected duty cycle of the data signal "with a predetermined duty cycle" (claim 1) by comparing the common-mode voltage of the data signal with a reference voltage 256.: "The difference between the common mode voltage of the input signal and a reference voltage is indicative of the difference between the duty cycle of the input signal and a predefined duty cycle." *Id.* ¶ [0038] The duty cycle detector 250-A thus is capable of determining "a first difference between the detected data signal duty cycle and the predetermined duty cycle," as claimed.

Furthermore, Figures 2A and 2B are linked by the skew values (e.g., SkA 216, SkB 218, etc) produced by the duty cycle detector 228 of Figure 2B and used by the clock duty cycle adjuster 214 of Figure 2A.

In some embodiments, the duty cycle detector 228 of Figure 2B provides as an output "one or more skew values (e.g., SkA 216, SkB 218, etc)" that correspond to "the difference between the data signal duty cycle and the predetermined duty cycle." *Id.* ¶ [0034]. These skew values 216 and/or 218 are provided to a clock duty cycle adjuster 214 of Figure 2A. A buffer 206 receives a system clock signal 204 and provides the system clock signal to the clock duty cycle adjuster 214. *Id.* ¶ [0031]. The clock duty cycle adjuster 214 "will typically generate a receiver clock signal based on the system clock signal." *Id.* ¶ [0040]. The clock duty cycle adjuster 214 uses the skew values 216 and/or 218 "for adjusting the receiver clock duty cycle." *Id.* ¶ [0035].

In conclusion, **the combination of structures in Figures 2A, 2B, and 2D described above provides one example of support for every limitation of claim 1.** Other examples are possible. As discussed, Figure 2A is linked to Figure 2B by skew values 216 and 218, and Figure 2D is linked to Figure 2B by the specification's statement that the duty cycle detector 250-A could be a data signal duty cycle detector. *See id.* ¶ [0038].

Furthermore, the phrase "the detected duty cycle" is not indefinite; it refers to the duty cycle of the data signal. The claim describes "*detecting* a duty cycle of a data signal" and "*receiving* a system clock signal." The prior use of "detecting" in the context of the data signal, but not in the context of the clock signal, indicates that "the *detected* duty cycle" is the duty cycle of the data signal.

Regarding claim 2, the Examiner again argued that "there is no circuit that detects 'duty cycle of a data signal' seen" and that the "detected duty cycle" was indefinite because it could refer to either the duty cycle of data signal or of the system clock. The Examiner also argued that "[i]t is not clear how this circuit can detect multiple data signals from multiple devices as recited."

As discussed above with regard to claim 1, the duty cycle detector 228 of Figure 2B detects the duty cycle of the data signal 226, and the phrase "detected duty cycle" refers to the duty cycle of the data signal.

Support for detecting multiple data signals from multiple devices is found in paragraph [0036] of the specification, which states that "[i]n some embodiments the device in which the receiver clock circuitry of Figs. 2A and 2B resides receives data signals from first and second devices." Paragraphs [0035] and [0036] discuss details of such an implementation, in accordance with some embodiments. Furthermore, Figure 1B illustrates how two devices (transmitters 102 and 110) can be connected to a single receiver device 104 via a single bus 112.

Regarding claim 6, the Examiner states that "the predetermined duty cycle" is indefinite because it is not clear whether this phrase "is the same or different than 'a predetermined duty cycle' on line 4 of claim 1." Applicants' use of "the" prior to the phrase "predetermined duty cycle" in claim 6 indicates that the "predetermined duty cycle" of claim 6 is the same as the "predetermined duty cycle" of claim 1. *See* MPEP 2173.05(f) ("A claim which makes reference to a preceding claim to define a limitation is an acceptable claim construction.").

Regarding claim 21, the Examiner states that "[i]t is not clear what are the: 'clock receiver,' 'a data signal duty cycle detector,' and 'a receiver clock generator' in the drawings." An example of a 'clock receiver' is buffer 206 in Figure 2A: "A system clock signal 204 is received in a buffer 206." Specification ¶ [0031]. An example of 'a receiver clock generator' is the clock duty cycle adjuster 214 in Figure 2A, which "will typically generate a receiver clock signal based on the system clock signal." *Id.* ¶ [0040]. While this quotation is from a discussion of Figure 2C, the common numbering of the clock duty cycle adjuster 214 indicates that it also applies to Figure 2A: "Like reference numerals designate like portions." *Id.* ¶ [0009]. An example of 'a data signal duty cycle detector' is the duty cycle detector 228 in Figure 2B. Thus, the combination of Figures 2A and 2B provides support for these claim limitations. As discussed above, the circuit shown in Figure 2B is

connected to the circuit shown in Figure 2A: the circuit of Figure 2B provides skews 216 and 218 to the circuit of Figure 2A.

Regarding claim 27, the Examiner states that the terms "a clock cycle detector" and "a second correction circuit" are indefinite. Claim 27 has been amended to clarify that the previously claimed "clock cycle detector" is a "clock duty cycle detector." For example, duty cycle detector 208 of Figure 2A "detects the duty cycle of the system clock signal." *Id.* ¶ [0031]. The "second correction circuit" of claim 27 is configured "to adjust the duty cycle of the receiver clock" in accordance with the difference signal generated by the clock cycle detector. Thus, in some embodiments, the second correction circuit corresponds to circuitry within the clock duty cycle adjuster 214: "Duty cycle detector 208 generates one or more duty cycle correction (DCC) values. . . . For example, Fig. 2A illustrates two such values – DCC A 210 and DCC B 212 – that are used by two sides of the clock duty cycle adjuster 214 in correcting the receiver clock duty cycle to match a predetermined duty cycle." *Id.* Thus, the specification supports claim 27 as amended.

Regarding claim 42, the Examiner states that "means" for receiving a system clock signal," "means for detecting a duty cycle of a data signal," and "means for generating a receiver clock signal" are indefinite. Examples of means for performing these functions are described above with regard to claim 1.

CLAIM REJECTIONS – 35 U.S.C. § 102

The Examiner rejected claims 1-4, 21-26, 34, 35, and 42 under 35 U.S.C. § 102(e) in view of Figure 5 of Desai. For a proper showing that Desai anticipates these claims, Desai must disclose all elements of each rejected claim. The rejected claims include independent claims 1, 21 and 42.

With respect to the "comparing" element of claim 1, it is noted that Desai's comparator 508 does not detect and compare duty cycles. In fact, the comparator 508 cannot receive any information concerning the duty cycle of the received serial data, because the sampling flip-flop 502 "retimes the serial data." Col. 3, lines 46-47. Thus, no information about the duty cycle of the received data propagates beyond the sampling flip-flop 502, making it impossible for any later circuit to detect the duty cycle. Furthermore, the reference pattern is a predetermined series of bits, not a predetermined duty cycle.

With respect to the "adjusting" element of claim 1, Desai does not disclose adjusting a duty cycle of a receiver clock. Instead, Desai teaches shifting, with respect to the serial data bits, the clocking provided by the clock generator 506 to the demultiplier 504. Thus, Desai adjusts the phase of the "word clock" produced by the clock generator, but does not change its duty cycle. In fact, at no point does Desai discuss detecting or adjusting a duty cycle. Instead, Desai discloses a deserializer circuit for framing parallel data, which adjusts the phase of a clock signal, but not its duty cycle.

Because Desai does not disclose "comparing," and "adjusting" duty cycles, Desai does not anticipate claim 1 or its dependent claims. Similarly, because Desai does not disclose circuitry to "generate a first difference signal representing a first difference between the first duty cycle and a first predetermined duty cycle," and to "adjust the duty cycle of the receiver clock signal," Desai does not anticipate claim 21, its dependent claims, or claim 42.

The phrase "duty cycle" is a term of art having a specific meaning in the field of electrical engineering. The Examiner cannot arbitrarily assign a term of art another meaning that is contrary to its standard usage in the field. *See* MPEP 2111.01.III ("The ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.). The Examiner's citation of prior art involving signal phase, and not of duty cycles, is improper.

CLAIM REJECTIONS – 35 U.S.C. § 103

The Examiner rejected claims 5, 13, 14, 18-20, and 39-41 under 35 U.S.C. § 103(a) in view of Figure 5 of Desai. These claims all depend on either claim 1 or claim 21. As discussed above, rejection of independent claims 1 and 21 in view of Desai is improper. Therefore, these rejections also are improper.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 843-4000, if a telephone call could help resolve any remaining items.

Respectfully submitted,

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